Iddq Testing for CMOS VLSI

Rochit Rajsuman

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Provides coverage of IDDQ testing, including discussion of the correlation between physical defects and logical faults, and how IDDQ testing detects these defects. This title presents information on test generation for IDDQ testing; use of stuck-at and random vectors for IDDQ testing; use of IDDQ testing in factory production lines; cost benefit analysis; instrumentation issues; off-chip and on-chip current senors; ATE interface; case studies with memories and microprocessors; and proposed IEE QTAG standards. It also supplies planning guidelines and optimization methods, together with numerous examples ranging from simple circuits to extensive case studies. It should be useful as a reference for designers and test engineers.

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